NEXT-GENERATION NANOSYSTEMS: A Q & A WITH MAX SHULAKER

By Anne Stuart | EECS

Max Shulaker, an expert on nanosystems exploiting emerging nanotechnologies, joined the EECS faculty in the fall of 2016. He is the Emmanuel E. Landsman (1958) Career Development Assistant Professor of Electrical Engineering and Computer Science and a principal investigator for both the Microsystems Technology Laboratories (MTL) and Research Laboratory of Electronics (RLE). At MIT, he is starting the Novel Electronic Systems (NOVELS) research group.

He received bachelor's, master's, and PhD degrees in electrical engineering from Stanford University. His PhD research on carbon nanotube-based transistors and circuits resulted in several firsts:

- the first digital systems built entirely using carbon nanotube field-effect transistors, or FETs (including the first carbon nanotube microprocessor),
- the first monolithic three-dimensional integrated circuits combining arbitrary vertical stacking of logic and memory, and
- the highest performance and highly-scaled carbon nanotube transistors to date.

At MIT, Shulaker is launching an experimental research program aimed at realizing his vision for the next generation of electronic systems based on transformational nanosystems, leveraging the unique properties of emerging nanotechnologies and nanodevices to create new systems and architectures with enhanced functionality and improved performance.

Shulaker was interviewed in his Building 39 office, which overlooks the ongoing construction for MIT.nano, the new nanoscale fabrication and characterization facility scheduled to open in 2018. He spoke about his past and current research, his new experimental program, and his early experience at MIT.

Q: How did you become interested in nanosystems and nanotechnologies?

A: I got interested in this area in a class on digital systems that I took freshman or sophomore year at Stanford. The professor talked about trying to make a computer out of carbon nanotubes. It seemed like a crazy idea, but I asked the professor if I could help, and he said "yes." That started close to a decade of working on carbon nanotubes. The more things I did in the lab, the more excited I became about the technologies. That's one reason I always encourage undergraduates to get involved in research — you never know when you will find your passion.

This work was exciting to me because it spanned all layers of the computing stack. I began focusing on the materials and carbon nanotube synthesis. Then we started looking at circuits. Then we started looking at systems. Then we starting looking at new applications. And now, my own PhD students are working on projects that span all those layers as well. They have to work on the new materials to build new circuits to enable new systems to demonstrate new applications.

When you add up all of the benefits across all these different layers, you aren't talking about 10 or 20 percent benefits anymore, but instead gains exceeding several orders of magnitude. This work has the potential to make a huge difference in the world, and it is why I — and my students — are so excited to be working on it.

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Q. You've said that the broader field of emerging nanotechnologies is both exciting and depressing. Can you explain?

A: Sure. It's exciting because of the promise we say that by using these new technologies, we can make chips that will be extremely fast *and* extremely energy-efficient. We can have sensors distributed all over the world. We can have chips in your body finding — and curing — diseases. And although these promises are exciting, they're also a little depressing, because while we talk about how these technologies will change the world, too often in the lab we only make a single device, or a single transistor. So there is a huge disconnect between the motivation that we use to drive this field of research, and what we actually show working in the lab.

My group is trying to bridge the gap between what we *say* these emerging nanotechnologies can enable and what we actually *demonstrate* in the lab. To do this, the group works on — out of necessity — many different aspects: some people focus more on design and simulation, while others are experimentalists and actually build the systems that we design.

Q: Tell me about your groundbreaking PhD research. How did you become interested in that subject? Did you expect the number of "firsts" your research generated, or were you surprised? What's been the result?

A: I did not know when I started undergrad that I was "meant" to do nanosystems. I got involved early in research, and tried out several different areas. It was only by doing and working in the lab that I found out what I didn't like, what I did like, and eventually, what I loved.

We were certainly happy to have a number of "firsts," but that was never the motivation to doing the work. I think the fact that we are working to define a new area of research — nanosystems — naturally makes the work new and, hopefully, interesting. While I found my own research during my PhD fascinating, I'm even more excited about the projects my students are working on. They are doing a fantastic job, and I'm eager to see all of the "firsts" they achieve.

Q: Have you actually launched your experimental program at MIT?

A: Yes. I feel tremendously lucky to have formed a group around an amazingly strong and talented group of core students. I guess it is a cliché to say that the best part of being a professor is working with students, but it really surprised me how true that has been. It's the students in my research group, it's the students in my classes. Thanks in large part to them, and thanks to the amazing amount of support I've gotten from MIT and other faculty here, as well as from our sponsors, our lab is up and running. My students are in the lab right now building the next generation of these nanosystems!

Q: Here's something you've said about your work: "While investigating new devices or new architectures separately can be beneficial, combining the 'right' devices, with the 'right' architectures, in the 'right' way, results in performance gains that far exceed the sum of their individual benefits, while simultaneously providing a rich set of enhanced functionality for applications that otherwise may not be feasible using traditional technologies." Could you talk about what you mean by the "right devices," the "right architectures," and the "right way"?

A: That's a very important question. To take a step back: if we want to understand how to improve computing, we have to know what are the obstacles we are facing today. And it turns out that part of the reason progress in computing is stalling is there aren't just one or two obstacles facing computing, but many. For example, the "power wall" stems from the fact that it is becoming increasingly difficult to shrink devices smaller, and the "memory wall" refers to how a computer today can spend the vast majority of its time and energy just moving data between memory and logic — and there are many more "walls."

Because there are many obstacles, it means that there cannot just be one solution. For instance, even if I create an amazing transistor, I would still face the memory wall, and visa-versa. So to realize really, really big gains — like orders-of-magnitude gains — in computing, just solving one problem isn't enough. Instead, we need to use better devices to build better systems to enable new applications. So device-level research cannot exist in a vacuum. When we work on new devices, we have to figure out which devices, or which "right" device, is going to enable us to not only solve the "power wall," but also enable us to build new system architectures — or the "right" system — to address the memory wall.

Q: Next, can you provide examples of enhanced functionality and improved performance?

A: We will have something published on this very shortly, and it is a fast-expanding thrust for our group. By leveraging the new fabrication techniques that some emerging nanotechnologies afford us, we can actually make 3D chips, skyscraper chips with multiple levels built one on top of the other. You can have sensing, data storage, and computation — all in one chip. That kind of chip, with fine-grained integration between these heterogeneous aspects of a system, can only be built using these new technologies. In fact, we are working in collaboration with Stanford University on a project which shows that this is the key to achieving the next 1,000X gain in energy efficiency.

Q: You've also been described as planning "to leverage the richness of new nanomaterials, new computing and memory technologies, and heterogeneous integration to enable new applications beyond the scope of traditional computing." Please talk more about some of these new nanomaterials and technologies — and, especially, their potential.

A: I like to say that my group is not "married" to any specific emerging nanomaterial or nanotechnology. Rather, we are pretty substrate-agnostic, and instead really try to figure out which material is going to enable which devices to enable which systems, and so on. That being said, since a key application thrust for us is computing, we do work heavily on carbon nanotubes, which are rolled-up sheets of graphene to form nanocylinders with diameters of only about 1 nanometer. As you can imagine, there are a whole host of amazing things you can do with a carbon nanotube. We've made state-of-the-art, very energy-efficient transistors using them and we are beginning to use them as physical nano-sized tubes, and so on.

We have been fortunate enough to also start collaborating with other faculty here at MIT who work with other types of nanomaterials, and we have been developing new systems and applications leveraging those materials also. Hopefully, you'll be able to read about these new ideas soon!

Q: You've also been described as having the ultimate goal of driving nanosystems "from concept to reality, resulting in hardware demonstrations of what future electronic systems might look like." How close are we to seeing nanosystems move from concept to reality? How will that happen?

A: It is actually a reality today. We can build and test these futuristic nanosystems, and perform certain tasks now that you simply cannot perform with conventional hardware today. We have also been extremely fortunate to develop a strong collaboration with Analog Devices, Inc. — which, by the way, has done a remarkable job of fostering truly innovative ideas and projects — and we are working hard to see just how far we can push these futuristic ideas into becoming reality.

Another important aspect is that what we work on is compatible with what exists in fabrication and design. We can build on top of any conventional silicon chip today, using the same tools and design infrastructure that already exists. This makes the barrier to introduction much lower. Who knows? Maybe one day, we will replace all of silicon. But to begin with, we don't need to do that.

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Q: Anything else you'd like to add?

A: Coming into MIT, I had a very clear notion of what I wanted my group to work on. But that's been turned on its head. I've been so lucky to interact with other faculty here who are unbelievably talented. Together, we've come up with some really cool new ideas and projects I could not have dreamed of even describing before.

For instance, we have been so fortunate to start working today with Sangeeta Bhatia's lab, developing new imaging and diagnostic modalities, which is something very removed from traditional "computing." [***Editor's Note:*** Sangeeta Bhatia, the John J. and Dorothy Wilson Professor at MIT's Institute for Medical Engineering and Science (IMES) and in EECS, is director of the MIT Laboratory for Multiscale Regenerative Technologies (LMRT).]

These fantastic collaborations allow us to still drive our core competency of computing, yet simultaneously explore how nanosystems can impact applications that lie beyond the scope of what we traditionally view as computing.

Editor's Note: Shulaker was the lead author of an article about development of a new 3-D computer chip, published in the journal Nature in July 2017. For more on that story, see news.mit.edu/2017/new-3-d-chip-combines-computing-and-data-storage-0705.